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LARGE-SIGNAL GaAs FET AMPLIFIER CAD PROGRAM

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Abstract

A CAD program for the design of multistage power GaAs FET amplifiers has been developed. The program is capable of analyzing the circuit performance of power amplifiers as a function of their input powers and frequency. Either graphic or printed output is available.

In an optimizing mode, the program returns the load and source admittance values for optimum power performance of FET devices.

The small-signal performance of multistage FET amplifiers (hybrid or monolithic) can be predicted to a high degree of accuracy by using the measured S-parameters of the devices and the various matching circuit elements. Many CAD programs are available for performing the necessary calculations. Power amplifiers, however, are more difficult to design since the circuit parameters of the devices become dependent on the power level. A number of approaches to the design problem have been reported in the literature. Most of these approaches, namely the ones based on the load-pull method,[1] require a large number of measurements and are therefore very difficult to use in a one-power-stage circuit design and next to impossible in multi-power-stage designs. Tajima et al.[2] have successfully used a FET circuit model to which power-dependent elements have been added, to predict the power performance of a power amplification stage.

We have utilized their power-dependent FET model (Fig. 1) and constructed a multimoded CAD program, LSFET. The program can operate in three modes, one of optimization and two of analysis. In the optimization mode, the program calculates, at each frequency and input power level, the source and load impedances necessary for optimum power performance of a power FET device. In the analysis modes, the program can analyze the nonlinear performance of either one or two power amplifier stages. The amplifiers in either case, however, can contain any number of driving stages provided they operate in the linear regime.

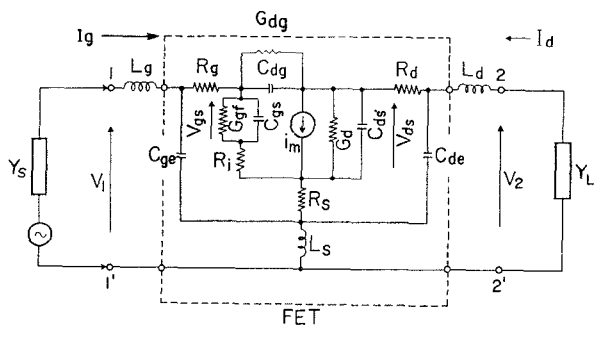

Fig. 1 GaAs FET large-signal equivalent circuit model.

The program accepts circuits whose block diagram is shown in Fig. 2. The input, interstage, and output matching networks can contain active or passive linear circuit elements whose parameters (S or Y) are calculated by other commercially available CAD programs (COMPACT for instance) and are written to files available to the nonlinear large-signal program.

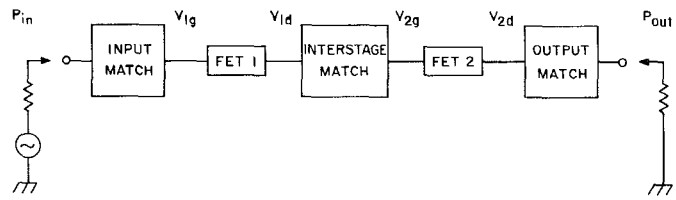

Fig. 2 Block diagram of FET amplifier with two power stages.

The FET parameters are stored in a data file. The file contains both the circuit elements shown in Fig. 1 and also the dc I-V curves, including breakdown characteristics, in parameter form. From the latter, the nonlinear g_m and g_d are calculated and their fundamental harmonic content used for the calculations. Our data files currently contain only FETs fabricated by our laboratory, for which we are able to obtain the complete necessary data.

The power calculation is performed by an iterative self-consistent method. Initially, a voltage v_{g2} is assumed. With this value, the nonlinear FET circuit elements and thereafter the voltage v_{d2} and current i_{d2} are calculated. Since the load across the FET is determined by the output matching network and the amplifier load, the ratio v_{d2}/i_{d2} is externally fixed. If this ratio does not agree with the ratio calculated from the nonlinear circuit model, v_{d2} is varied until a self-consistency is achieved. The whole process is repeated for the first power stage. Typically the convergence is fast.

The large-signal program, LSFET, is very easy to use. Prior to an analysis session, the parameters of the devices have to be resident in a library file, and the circuit descriptions of the various matching networks, as well as the frequency information, written into separate files. LSFET can interact with any program that is capable of calculating the necessary linear parameters. For our internal use, we have standardized on using the Y-parameters as calculated by the commercially available COMPACT program.

A sample analysis of a two-stage amplifier is shown in Figs. 3 and 4. In Fig. 3 the user's responses are underlined. From the presence of three file names on the first line, the program understands that an analysis of a two-stage design is called for. Two file names or none would have called for an analysis of a one-stage design or for an optimization.

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BEGIN,,LSFET   ,DRI5IN,DRI5TR,DRI5OT
   82/03/18.   09.12.24.

 ENTER DEVICES CODES:       FIRST STAGE FOLLOWED BY CR. THEN
                            SECOND STAGE FOLLOWED BY CR.
 CR ALONE IF YOU WANT TO TYPE IN THE DEVICES PARAMETERS
? MM
? NN
 PRINT COMPACT SOURCE,INTERSTAGE AND LOAD FILES ?
 PRINT Y PARAMETERS GENERATED BY ABOVE FILES? (YY,YN,NY,NN=CR)?  NN




   82/03/18.   09.14.44.

LARGE SIGNAL ANALYSIS, TWO STAGE AMPLIFIER

FET PARAMETERS                                                         FIRST STAGE FET            SECOND STAGE FET
(I) LINEAR ELEMENTS
     GATE,DRAIN,SOURCE RESISTANCES(OHM)                                 4.00 4.00 3.00             2.50 2.50 2.60
     GATE,DRAIN,SOURCE INDUCTANCES(NH)                                  0.00 0.00  .02             0.00 0.00  .02
     DRAIN-SOURCE,DRAIN-GATE,GATE PAD,DRAIN PAD CAPACITANCES"(PF)        .04  .02 0.00 0.00         .07  .02 0.00 0.00
     TRANSCONDUCTANCE TIME CONSTANT(PS)                                  .36                        .50
(II) DRAIN CURRENT PARAMETERS
     MAX DRAIN CURRENT(MA),KNEE AND PINCHOFF VOLTAGE(V)                  60.  .50 2.80             100.  .50 2.80
     PARAMETERS A,B,N,W                                                 -.20  .10 2.00  .50        -.20  .10 2.00  .50
     RESIDUAL DRAIN CONDUCTANCE(MS),PINCHOFF INCREMENT FACTOR           1.75  .12                  3.05  .12
(III) GATE PARAMETERS (VPHI=0.8V)
     SCHOTTKY SATURATION CURRENT(PA),ZERO BIAS GATE CAPACITANCE(PF)     5.00  .40                 10.00  .55
     ALP(Q/NKT), GATE CHARGING TIME CONSTANT(PS,RI*CGS)               30.00 1.80                  30.00 1.17
(IV) BREAKDOWN PARAMETERS
     BREAKDOWN VOLTAGE(V),INCREMENT RESISTANCE(OHM)                    15.00 75.00                  15.00 37.00
     BREAKDOWN RESISTANCE,INCREMENT FACTOR(OHM)                       400.   1600.                200.    800.

 "FIRST STAGE BIAS VGS,VDS(V)= "  ?  -1.5  7
 "SECOND STAGE BIAS VGS2,VDS2(V)= " ? -1.5 7
 II: NUMBER OF GATE RF VOLTAGE INCREMENTS ?  40
```

Fig. 3 Sample LSFET input instructions and device parameter listings. User's responses are underlined.

FREQUENCY(GHZ)=12.00

SMALL SIGNAL PERFORMANCE

	S11(MAG,DEG)		S12(MAG,DEG)		S21(MAG,DEG)		S22(MAG,DEG)		MAG MSG(DB)	K	S21(DB)
FIRST STAGE FET	.759E+00	-.860E+02	.693E-01	.478E+02	.110E+01	.113E+03	.797E+00	-.231E+02	10.547	1.056	.799
SECOND STAGE FET	.787E+00	-.106E+03	.800E-01	.385E+02	.138E+01	.994E+02	.680E+00	-.423E+02	12.357	.831	2.780
AMPLIFIER	.357E+00	-.171E+03	.109E-01	-.261E+02	.296E+01	.999E+02	.246E+00	-.718E+02	10.317	12.673	9.433

LARGE SIGNAL PERFORMANCE

PIN (DBM)	POUT (DBM)	GAIN (DB)	PAE (PCENT)	GGF (S)	CGS (PF)	RI (OHM)	GM (S)	GD (S)	GDG (S)	IDS (MA)	IDG (MA)	IGS (MA)	V1 (V,DEG)		V2 (V,DEG)	
0.00	0.00	0.00	0.00	.562E-29	.236E+00	.762E+01	.197E-01	.175E-02	0.	26.	0.00	.00	.05	16.	.05	164.
				.112E-28	.325E+00	.360E+01	.325E-01	.305E-02	0.	43.	0.00	.00	.05	13.	.07	156.
-8.65	1.34	9.99	.26	.120E-27	.236E+00	.762E+01	.201E-01	.175E-02	0.	26.	0.00	.00	.23	15.	.16	-131.
				.176E-27	.325E+00	.360E+01	.342E-01	.305E-02	0.	43.	0.00	.00	.22	11.	.65	-173.
-2.61	7.26	9.87	.99	.273E-25	.237E+00	.760E+01	.201E-01	.175E-02	0.	26.	0.00	.00	.46	15.	.32	-131.
				.260E-25	.325E+00	.360E+01	.339E-01	.305E-02	0.	43.	0.00	.00	.43	11.	1.28	-173.
.97	10.75	9.79	2.18	.101E-22	.238E+00	.757E+01	.200E-01	.175E-02	0.	26.	0.00	.00	.69	16.	.49	-131.
				.577E-23	.327E+00	.358E+01	.337E-01	.305E-02	0.	44.	0.00	.00	.65	11.	1.91	-173.
3.55	13.24	9.69	3.78	.496E-20	.239E+00	.752E+01	.199E-01	.175E-02	0.	27.	0.00	.00	.93	16.	.66	-131.
				.152E-20	.328E+00	.356E+01	.336E-01	.305E-02	0.	45.	0.00	.00	.86	12.	2.55	-173.
5.60	15.18	9.58	5.75	.320E-17	.241E+00	.746E+01	.198E-01	.175E-02	0.	27.	0.00	.00	1.18	16.	.83	-130.
				.440E-18	.331E+00	.354E+01	.336E-01	.305E-02	0.	46.	0.00	.00	1.08	12.	3.19	-173.
7.33	16.76	9.43	8.01	.280E-14	.244E+00	.737E+01	.196E-01	.175E-02	0.	28.	0.00	.00	1.43	16.	1.01	-130.
				.135E-15	.334E+00	.351E+01	.336E-01	.305E-02	0.	47.	0.00	.00	1.29	12.	3.82	-173.
8.88	18.11	9.23	10.50	.357E-11	.249E+00	.724E+01	.194E-01	.175E-02	0.	29.	0.00	.00	1.70	16.	1.21	-130.
				.434E-13	.338E+00	.347E+01	.336E-01	.305E-02	0.	49.	0.00	.00	1.51	12.	4.46	-173.
10.32	19.28	8.96	13.11	.754E-08	.255E+00	.705E+01	.191E-01	.175E-02	0.	30.	0.00	.00	1.98	16.	1.42	-129.
				.143E-10	.343E+00	.341E+01	.337E-01	.305E-02	0.	50.	0.00	.00	1.73	12.	5.11	-173.
10.71	19.54	8.83	13.72	.656E-07	.258E+00	.699E+01	.191E-01	.175E-02	0.	31.	0.00	.00	2.06	16.	1.48	-129.
				.614E-10	.344E+00	.340E+01	.337E-01	.305E-02	.96E-05	51.	.03	.00	1.78	12.	5.26	-173.
11.08	19.78	8.70	14.30	.530E-06	.260E+00	.692E+01	.190E-01	.175E-02	0.	31.	0.00	.00	2.13	16.	1.54	-129.
				.263E-09	.346E+00	.338E+01	.337E-01	.305E-02	.28E-04	51.	.10	.00	1.83	12.	5.41	-173.
11.45	20.00	8.54	14.85	.451E-05	.263E+00	.683E+01	.189E-01	.175E-02	0.	32.	0.00	.00	2.21	16.	1.61	-129.
				.113E-08	.347E+00	.337E+01	.336E-01	.305E-02	.51E-04	51.	.19	.00	1.89	12.	5.55	-173.
11.86	20.21	8.34	15.36	.407E-04	.267E+00	.674E+01	.188E-01	.175E-02	0.	32.	0.00	.04	2.29	16.	1.68	-129.
				.485E-08	.349E+00	.335E+01	.336E-01	.305E-02	.76E-04	51.	.30	.00	1.94	12.	5.68	-173.
12.44	20.40	7.96	15.73	.392E-03	.271E+00	.663E+01	.187E-01	.175E-02	0.	33.	0.00	.44	2.39	16.	1.75	-130.
				.209E-07	.351E+00	.333E+01	.335E-01	.305E-02	.10E-03	51.	.41	.00	2.00	12.	5.81	-173.
12.92	20.48	7.57	15.68	.995E-03	.273E+00	.660E+01	.187E-01	.175E-02	0.	33.	0.00	1.12	2.44	16.	1.77	-130.
				.374E-07	.352E+00	.332E+01	.335E-01	.305E-02	.11E-03	51.	.43	.00	2.02	12.	5.87	-173.
13.81	20.55	6.75	15.24	.248E-02	.274E+00	.656E+01	.187E-01	.175E-02	0.	33.	0.00	2.84	2.52	16.	1.80	-130.
				.671E-07	.353E+00	.331E+01	.335E-01	.305E-02	.12E-03	51.	.50	.00	2.04	12.	5.91	-173.
14.54	20.63	6.09	14.80	.389E-02	.275E+00	.655E+01	.186E-01	.175E-02	0.	33.	0.00	4.48	2.58	16.	1.82	-130.
				.120E-06	.354E+00	.330E+01	.335E-01	.305E-02	.13E-03	51.	.53	.00	2.06	12.	5.97	-173.
14.54	20.64	6.10	14.90	.389E-02	.275E+00	.655E+01	.186E-01	.175E-02	0.	33.	0.00	4.48	2.58	16.	1.82	-130.
				.139E-06	.354E+00	.330E+01	.334E-01	.305E-02	.14E-03	51.	.58	.00	2.07	12.	5.97	-173.

Fig. 4 Sample LSFET printed output.

Following the three self-explanatory opening questions, the program prints the parameters and equivalent circuit values of the selected devices. Bias information and the number of desired input power increments at each frequency are then supplied. A sample analysis, repeated at each frequency, is shown in Fig. 4. The program calculates the small-signal performance and follows by the large-signal analysis. As can be seen in the figure, all the power-dependent elements of the equivalent circuits of the two devices are printed at each power level (columns 5 through 13), the elements of FET1 in the first line, of FET2 in the second. In the first four columns, the input and output powers, the gain and power-added efficiency of the amplifier are printed.

The drain and gate currents, I_D and I_G are defined as positive when they flow into the terminals of the FET.

$$I_D = I_{DS} + I_{DG}$$

$$I_G = I_{GS} - I_{DG}$$

where I_{DS}, I_{DG}, and I_{GS} are given in columns 11, 12 and 13. The presence of gate current indicates the onset of power saturation. The direction of I_G identifies the power-limiting factor; positive I_G indicates the Schottky junction breakdown, while negative I_G is caused by forward conduction. The voltages V_1 and V_2 are defined in Figs. 1 and 2. Graphic representation of each parameter, as a function of frequency, is also available. Since the program uses nonlinear analysis, the input power increments are not regular. An interpolating routine is therefore also available.

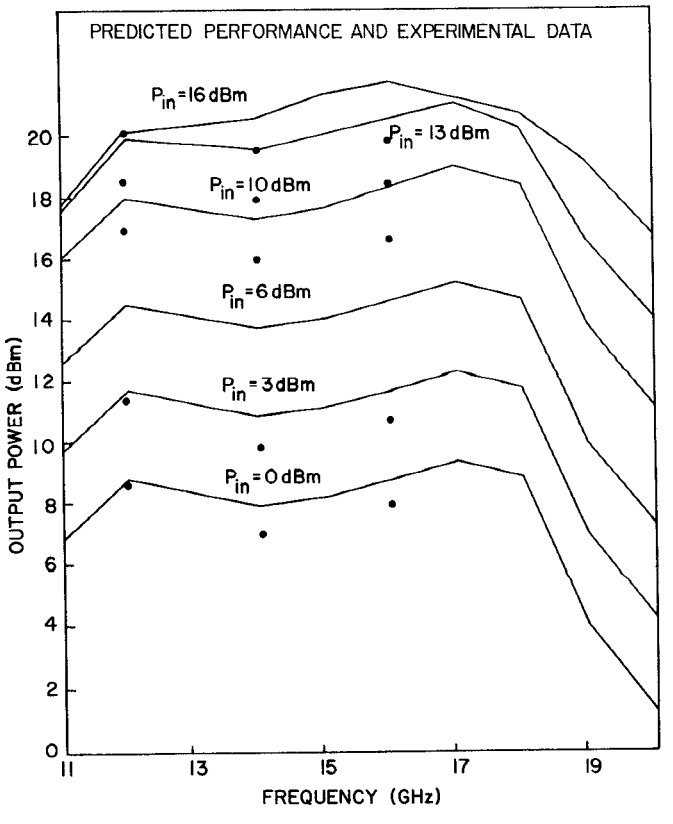

Fig. 5 Ku-band amplifier. Experimental data for P_{in} = 0, 3, 10, 13, 16 dBm.

A sample graphic representation is shown in Fig. 5. The figure shows the predicted power performance of a Ku-band monolithic amplifier fabricated at our laboratory, at various power levels as a function of frequency, and the measured performance at several points. The measured data is shown as measured, with jig losses included. The agreement between the predicted and actual performances is quite good.

Typically, our circuit design philosophy follows the steps shown in Fig. 6. We use our large-signal program only after a small-signal design has been performed. In the small-signal design, however, we constrain the impedance levels presented to the FETs to the values dictated by the large-signal requirements. To obtain these values, our large-signal program is run in its optimizing mode in which case it prints the optimum loads required for the maximum designed power. Once these loads are known, the design of the input, interstage, and output matching network can be done in a straightforward manner using available CAD programs. Numerous network topologies will provide suitable small-signal performance. From our design experience, however, we found that several of them will provide very poor high-power performance; several design iterations are typically necessary until both a small-signal and a large-signal design can be simultaneously achieved. To the latter end, our large-signal analysis has proven to be extremely valuable.

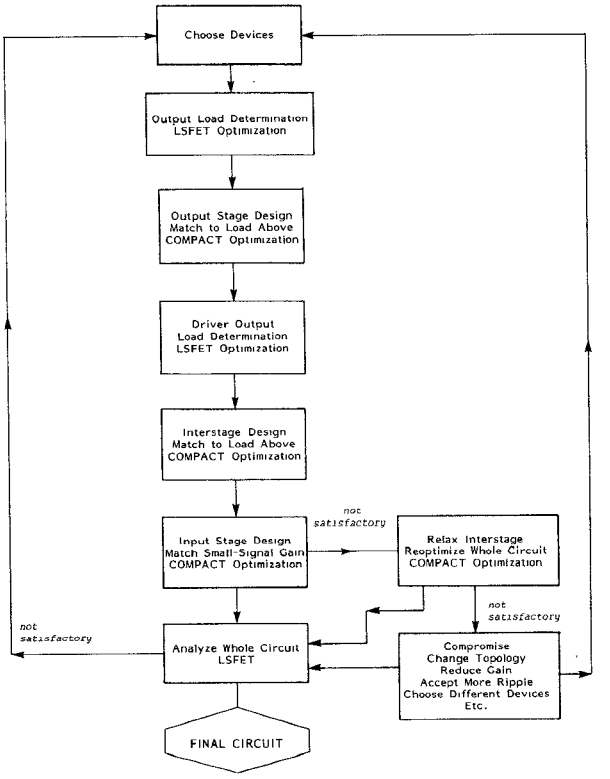

Fig. 6 Multistage power amplifier design steps.

References

1. J. E. Degenford et al., "A study of optimal matching circuit topologies for broadband monolithic power amplifiers," 1981 IEEE MTT-S International Microwave Symposium Digest, p. 351.

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